MULTIPLE ON-CHIP TEST RUNS AND REPAIRS FOR MEMORIES

Abstract of the Disclosure

A structure and method for performing on-chip test runs and repairs of a memory chip. In the first test run and repair, a BIST circuit obtains the original combined repair solution from a fuse bay on the memory chip, runs the first test run for the memory chip, obtains a first test-run repair solution, and combines the original combined repair solution and the first test-run repair solution to obtain the latest/first combined repair solution. Then, an exclusive-OR gate is used to compare the first combined repair solution and the original combined repair solution to obtain a first new repair solution, which is programmed into the fuses of the fuse bay. As a result, the fuse bay stores the first combined repair solution. In the second test run and repair, a similar process is performed, and so on. As a result, any number of test runs and repairs can be performed on-chip for the memory chip.